**Semiconductor Section Outline**

**1. Fundamentals of Semiconductors**

**1.1 The Importance of Tunable Resistivity**

* **Basic Resistance Equation**: R = ρL/A
  + Where ρ is resistivity, L is length, and A is cross-sectional area
* **Three ways to modify resistance**:
  + Change physical dimensions (length or area)
  + Change resistivity through chemical composition
  + Modify resistivity through electromagnetic fields
* **Unique semiconductor property**: Ability to dynamically tune resistivity by controlling charge carrier density
  + Metals: Fixed carrier density (~10²²-10²³/cm³)
  + Insulators: Very low carrier density (~10⁻⁵⁷/cm³)
  + Semiconductors: Tunable carrier density (~10¹⁰-10²⁰/cm³)

**1.2 Applications of Tunable Resistivity**

* **Digital logic**: Creating electronic switches
* **Analog circuits**: Signal amplification
* **Power electronics**: AC voltage rectification
* **Other applications**: Sensing, power generation, light emission/detection

**1.3 Semiconductor Materials**

* **Elemental semiconductors**: Silicon (Si), Germanium (Ge), Carbon (diamond)
* **Binary compounds**: GaAs, InSb, SiC, CdSe
* **Ternary compounds**: AlGaAs, InGaAs

**1.4 Silicon Crystal Structure**

* Silicon forms a diamond cubic structure
* Each Si atom bonds with four nearest neighbors
* Lattice constant: 5.43 Å
* Si belongs to Group IV of the periodic table with 4 valence electrons

**2. Charge Carriers in Semiconductors**

**2.1 Bond Model and Charge Carriers**

* Electrons in silicon are bound in covalent bonds
* When a bond breaks:
  + A conduction electron is created (mobile negative charge)
  + A hole is created (mobile positive charge)
* Both electrons and holes contribute to current flow

**2.2 Doping and Carrier Control**

* **N-type doping**:
  + Adding Group V elements (e.g., Arsenic)
  + Introduces extra electrons as majority carriers
  + These dopants are called "donors"
* **P-type doping**:
  + Adding Group III elements (e.g., Boron)
  + Creates holes as majority carriers
  + These dopants are called "acceptors"
* Doping allows precise control of semiconductor conductivity

**2.3 Compound Semiconductors (GaAs)**

* GaAs has the same crystal structure as Silicon
* Made from Group III (Ga) and Group V (As) elements
* Important for optoelectronic applications
* Different doping considerations compared to elemental semiconductors

**3. Energy Band Theory**

**3.1 Energy Band Diagram**

* **Conduction Band (Ec)**: Energy level where electrons can move freely
* **Valence Band (Ev)**: Energy level of bound electrons
* **Band Gap (Eg)**: Energy separation between bands
  + Si: 1.12 eV
  + GaAs: 1.42 eV
  + Diamond: 6.0 eV

**3.2 Material Classification by Band Structure**

* **Conductors**: Partially filled bands allow easy electron movement
* **Semiconductors**: Moderate band gap (typically < 3eV)
* **Insulators**: Large band gap (> 4eV)

**3.3 Measuring Band Gap**

* Band gap can be determined by the minimum energy of photons absorbed
* When photon energy (hν) ≥ Eg, electrons can be excited from the valence to conduction band

**4. P-N Junction Diodes**

**4.1 Diode Fundamentals**

* Junction between p-type and n-type semiconductors
* Exhibits rectifying behavior (conducts current in one direction)
* Consists of anode (p-side) and cathode (n-side)

**4.2 Diode Operating Modes**

* **Forward bias**:
  + P-side connected to positive terminal, N-side to negative
  + Reduces barrier potential, allowing current flow
  + "Open door" condition
* **Reverse bias**:
  + P-side connected to negative terminal, N-side to positive
  + Increases barrier potential, blocking current flow
  + "Closed door" condition
  + Creates a depletion region

**4.3 Diode Equation**

* **Ideal Diode Equation**: I = I₀(e^(qV/kT) - 1)
  + I₀ is the reverse saturation current
  + q is the electron charge
  + V is the applied voltage
  + k is Boltzmann's constant
  + T is temperature in Kelvin
* **Non-Ideal Diode Equation**: I = I₀(e^(qV/nkT) - 1)
  + n is the ideality factor (n > 1 for non-ideal diodes)

**5. Transistors**

**5.1 Historical Development**

* First transistor (point-contact): 1947 by Bardeen, Brattain, and Shockley at Bell Labs
* 1956 Nobel Prize in Physics awarded for the transistor invention
* Field-Effect Transistor (FET) concept patented by Oskar Heil in 1935
* Working MOSFET demonstrated in 1955

**5.2 MOSFET Fundamentals**

* **Structure**: Source, Drain, Gate, and Channel regions
* **Working principle**: Applying voltage to gate controls current flow between source and drain
* **Types**:
  + NMOS (n-channel): Uses electrons as carriers
  + PMOS (p-channel): Uses holes as carriers

**5.3 MOSFET Operation Modes**

* **Cutoff region**: VG < VT, minimal current flow
* **Linear region**: VG > VT and small VDS, current increases with VDS
* **Saturation region**: VG > VT and VDS > VDS,sat, current reaches maximum
* **Channel pinch-off**: Occurs when VDS = VG - VT, creating saturation condition

**5.4 MOSFET Current Equations**

* **Linear region**: ID = (Zμn/L)Cox[(VG-VT)VDS - VDS²/2], for 0 < VDS < VDS,sat
* **Saturation region**: ID,sat = (Zμn/2L)Cox(VG-VT)², for VDS > VDS,sat
* Cox is oxide capacitance per unit area (Cox = εox/xox)

**5.5 Subthreshold Conduction**

* Current flow when VG < VT
* Important for power consumption in digital circuits
* Increases exponentially with VG
* The current at VGS=0 and VDS=VDD is called Ioff (leakage current)

**6. CMOS Technology**

**6.1 Complementary MOSFETs**

* Combines both NMOS and PMOS devices
* **NMOS**: Conducts when gate voltage is high
* **PMOS**: Conducts when gate voltage is low

**6.2 CMOS Inverter**

* **Structure**: PMOS and NMOS in series between VDD and ground
* **Operation**:
  + When input is high (VDD): NMOS conducts, PMOS blocks → output is low (0V)
  + When input is low (0V): PMOS conducts, NMOS blocks → output is high (VDD)
* **Advantages**: Low power consumption, high noise immunity

**6.3 NMOS vs. PMOS Performance**

* PMOS devices have approximately half the current drive of NMOS
* Due to lower hole mobility compared to electron mobility
* Requires careful design considerations in circuit implementation

**7. Advanced Concepts**

**7.1 Channel Length Effects**

* Short channel devices (ΔL ~ L) show less ideal behavior
* Long channel devices (ΔL << L) follow square law more closely

**7.2 Threshold Voltage**

* Voltage required to form a conduction channel
* Determined by semiconductor doping, oxide thickness, and other parameters
* Can be extracted from ID-VGS characteristics

**7.3 Mobility Degradation**

* Carrier mobility decreases at high gate voltages
* Causes deviation from ideal square law behavior
* Important consideration in advanced device modeling